layer, said gate regions electrically connected together;

forming a pattern of recesses extending from the second surface of the substrate into interior portions of the semiconductor substrate, said recesses located at chosen positions and having chosen shapes and chosen depths in the substrate; and

forming resistivity-lowering bodies in the recesses, the resistivity-lowering bodies comprising a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.

77. A method according to Claim 52 wherein the step of forming the pattern of recesses comprises sawing or etching a recess into the surface of the substrate.

78. A method according to Claim 52 wherein the step of forming the pattern of recesses comprises laser etching to form cylindrical recesses.

79. A method according to Claim 76 wherein the step of forming the pattern of recesses comprises forming a repeated pattern.

80. A method according to Claim 79 wherein the repeated pattern is a trapezoidal pattern.

81. A method according to Claim 76 wherein the recesses comprises a grid of intersecting trenches.

82. A method according to Claim 76 further comprising forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one resistivity-lowering body.

83. A method according to Claim 76 wherein forming the at least one resistivity-lowering body comprises filling an associated recess.

84.(amended) A method according to Claim 76 further comprising forming a barrier layer lining in at least one recess.

85.(amended) A method according to Claim 76 wherein forming the resistivity-lowering body comprises forming said body using an electrical conductor having an electrical resistivity less than about 10^{-4} Ω•cm.

86.(amended) A method according to Claim 76 wherein forming the recesses and associated resistivity-lowering body comprises forming the recesses and the assoicated resistivity lowering bodies to define a proportion of the semiconductor substrate area adjacent the at least one device active region no less than about 0.4 percent.

87.(amended) A method according to Claim 76 wherein forming the recesses and associated resistivity-lowering body comprises forming the recesses and the associated resistivity lowering bodies to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

88. A method according to Claim 76 wherein forming the at least one recess and associated resistivity-lowering body comprises forming an array of recesses and associated resistivity-lowering bodies.

89.(amended) A method according to Claim 88 wherein forming the array of recesses and associated resistivity-lowering bodies comprises are arranged in a grid pattern.

90. A method according to Claim 89 wherein forming the grid pattern comprises cutting trenches in the second surface of the semiconductor substrate.

91. A method according to Claim 76 wherein forming the at least one device active region comprises forming at least one device active region for a metal-oxide semiconductor field-effect transistor (MOSFET).

92. A method according to Claim 76 wherein forming the at least one device active region comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

93. A method according to Claim 76 wherein forming the at least one device active region comprises forming at least one active region of a microprocessor.

94.(amended) A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising:

in the substrate forming a drain layer of a first polarity;

in a first surface, forming one or more well regions above the drain layer and comprising dopants of a second and opposite polarity;

in the first surface and in said well regions, forming source regions of dopants of the first polarity, the source regions laterally spaced from each other;

forming gate regions over portions of the well regions between the source regions and the drain layer; and

in the second surface of the substrate forming one or more resistivity-lowering bodies extending from the second surface of the substrate into interior portions of the semiconductor substrate, the resistivity-lowering bodies comprising a material different than the semiconductor substrate and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.

95. A method according to Claim 94 further comprising forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one resistivity-lowering body.

96. A method according to Claim 94 wherein the at least one resistivity-lowering body comprises an electrical conductor having an electrical resistivity less than about 10^{-4} Ω•cm.

97. A method according to Claim 94 wherein the resistivity-lowering body comprises forming the resistivity-lowering body to define a proportion of the semiconductor substrate area adjacent the at least one device active region not less than than about 0.4 percent.

98. A method according to Claim 94 wherein the resistivity-lowering body extends into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

99. A method according to Claim 94 wherein forming the at least one resistivity-lowering body comprises forming an array of resistivity-lowering bodies.

100. A method according to Claim 99 wherein the array of resistivity-lowering bodies comprises a grid pattern.

101. A method according to Claim 100 wherein forming the grid pattern comprises cutting trenches in the second surface of the semiconductor substrate.

102. A method according to Claim 94 wherein forming the at least one device active region comprises forming at
least one device active region for a metal-oxide semiconductor field-effect transistor (MOSFET).

103. A method according to Claim 94 wherein forming the at least one device active region comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

104. A method according to Claim 94 wherein forming the at least one device active region comprises forming at least one active region of a microprocessor.

REMARKS

This amendment is submitted in response to the office action mailed August 9, 2001. The application was unintentionally abandoned. A petition to revive is submitted